

67,200-974
2002-0306

ABSTRACT OF THE DISCLOSURE

A semiconductor wafer is disclosed that includes a plurality of fields, including a plurality of alignment fields. Each alignment field includes a plurality of intra-field small scribe lane primary mark (SSPM) overlay mark pairs there around. The SSPM mark pairs allow for in-situ, non-passive intra-field alignment correction. In one embodiment, there may be between two and four alignment fields, and between two and four SSPM mark pairs around each alignment field. The SSPM marks of each mark pair may be extra scribe-lane marks.